**Amendments to the Specification:**

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Please replace paragraph [00~~63~~47] with the following rewritten paragraph:

-- [00~~63~~47] Anti-fuse transistor **100** includes a variable thickness gate oxide **102** formed on the substrate channel region **104**, a polysilicon gate **106**, sidewall spacers **108**, first and second diffusion regions **110** and **112** respectively, and LDD regions **114** in each of the diffusion regions **110** and **112**. <u>Field oxide regions **113** are grown adjacent to the diffusion regions **110** and **112**, and surrounds the channel region **104** and the diffusion regions **110** and **112**, to isolate the anti-fuse transistor **100** from adjacent anti-fuse transistors or other transistor structures</u>. The variable thickness gate oxide **102** consists of a thick oxide and a thin gate oxide such that a portion of the channel length is covered by the thick gate oxide and the remaining portion of the channel length is covered by the thin gate oxide. Generally, the thin gate oxide edge meeting diffusion region **112** defines a fusible edge where oxide breakdown can occur. The thick gate oxide edge meeting diffusion region **110** on the other hand, defines an access edge where gate oxide breakdown is prevented and current between the gate **106** and diffusion region **110** is to flow for a programmed anti-fuse transistor. While the distance that the thick oxide portion extends into the channel region depends on the mask grade, the thick oxide portion is preferably formed to be at least as long as the minimum length of a high voltage transistor formed on the same chip. --

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Please replace paragraph [00~~72~~56] with the following rewritten paragraph:

-- [00~~72~~56] Figure 6a shows an anti-fuse transistor 200 having an "L" shaped gate/diffusion perimeter, also referred to as the fusible edge, at the floating diffusion end of the device. Anti-fuse transistor **200** is essentially the same as anti-fuse transistor **100** shown in Figures 4 and 5. An active region **202** has a diffusion region with bitline contact **204**, and a polysilicon gate **206** formed over a variable thickness gate oxide layer (not shown). The OD2 mask **208** defines where the thick gate oxide is formed underneath polysilicon gate **206**. In the present embodiment, the floating diffusion region, channel region, and polysilicon gate share a common "L" shaped edge. The edge consists of two edge segments <u>**209**</u> oriented at an angle with respect to each other. While the presently

shown embodiment shows the angle to be about 90 degrees, the angle can be set to 135 degrees if desired. –

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Please replace paragraph [00~~73~~] with the following rewritten paragraph:

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--[00~~73~~] Figure 6b shows an anti-fuse transistor **210** having a straight "S" shaped gate/diffusion perimeter, also referred to as the fusible edge, at the floating diffusion end of the device. Anti-fuse transistor **210** is essentially the same as anti-fuse transistor **200** shown in Figure 6a. An active region **202** has a diffusion region with bitline contact **204**, and a polysilicon gate **206** formed over a variable thickness gate oxide layer (not shown). The OD2 mask **208** defines where the thick gate oxide is formed underneath polysilicon gate **206**. In the present embodiment, the floating diffusion region, channel region, and polysilicon gate share a common straight "S" shaped edge. The edge consists of three edge segments **209** oriented at 90 degree angles with respect to each other. --

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Please replace paragraph [00~~86~~] with the following rewritten paragraph:

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-- [00~~86~~] Figure 11a illustrates a plurality of anti-fuse transistor memory cells arranged in a basic cross-point array, according to an embodiment of the present invention. Sensing is single ended in the present embodiment. The anti-fuse transistor memory array **700** includes anti-fuse transistors **702** coupled to wordlines WL0-WL3 and bitlines BL0, BL1, BL2 and BL3. Anti-fuse transistors **702** can be implemented with any of the previously described anti-fuse transistors. Each bitline is connected to a p-channel isolation transistor **704**, which in turn is connected to thin gate oxide p-channel pass gates **706, 708, 710** and **712**. It is noted that isolation transistors **704** are thick gate oxide transistors, where this thick gate oxide can be the same combination of the intermediate oxide and the thin gate oxide used for the anti-fuse transistor embodiments of the present invention. The gate terminal of all isolation transistors **704** receive isolation voltage VB, while the gate terminals of pass gates **706**, **708**, **710** and **712** receive column select signals Y0, Y1, Y2 and Y3 respectively. The column select signals perform a one of four bitline selection to couple one of the bitlines to cross-point sense amplifier **714**. Cross-point sense amplifier **714** can be a current sense amplifier that

compares the current of the bitline to a reference current IREF, and generally denotes single-ended sensing schemes in the present description, where a bitline voltage or current is compared to a reference signal carried on another line. –

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Please replace paragraph [00~~96~~81] with the following rewritten paragraph:

– [00~~96~~81] Figure 13 shows a folded bitline architecture employing the previously described anti-fuse transistors **702**. Memory array **800** is similar to memory array **700** of Figure 11b, except that memory cells **702** are arranged in the folded bitline architecture. Figure 13 includes a wordline decoder circuit 718 for driving wordlines WL0 to WL3. Those skilled in the art will understand that the decoding circuitry within wordline decoder circuit 718 can include any configuration of logic gates and circuits for driving one wordline in response to a row address.–